CLAIMS

1. A memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent is capable of selectively mapping one or more of the first lanes to one or more of the second lanes.

2. A memory agent according to claim 1 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

3. A memory agent according to claim 1 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

4. A memory agent according to claim 1 wherein the memory agent may selectively map one or more of the first lanes to one or more of the second lanes during a lane testing operation.

5. A memory agent according to claim 1 wherein the memory agent may selectively map one or more of the first lanes to one or more of the second lanes according to a plurality of mappings.

6. A memory agent according to claim 1 wherein the memory agent may selectively map one or more of the first lanes to one or more of the second lanes responsive to a training sequence received on the first link interface.

7. A memory agent according to claim 6 wherein the memory agent may retransmit the training sequence through the second link interface.

8. A memory agent according to claim 1 wherein the memory agent comprises a memory buffer.

9. A memory agent according to claim 1 wherein the memory agent comprises a memory module.

10. A memory agent according to claim 1 wherein the memory agent comprises a loopback unit.

11. A memory agent according to claim 1 wherein the loopback unit comprises a multiplexer.

12. A memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent may:

transmit training sequences having different mapping indicators on one or more of the first lanes;

receive return sequences on one or more of the second lanes responsive to the training sequences; and

analyzing the return sequences to identify failed lanes.

13. A memory agent according to claim 12 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

14. A memory agent according to claim 12 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

13. A memory agent according to claim 12 wherein the memory agent may identify whether a failed lane is a first lane or a second lane.

14. A memory agent according to claim 12 wherein the memory agent may transmit test parameters in the training sequences.

15. A memory agent according to claim 12 wherein the memory agent may transmit electrical stress patterns in the training sequences.

16. A memory agent according to claim 12 wherein the memory agent comprises a memory controller.

17. A method comprising:

transmitting a first training sequence to a memory agent on a first plurality of lanes;

transmitting a first return sequence from the memory agent on a second plurality of lanes responsive to the first training sequence according to a first mapping;

transmitting a second training sequence to the memory agent on a third plurality of lanes; and

transmitting a second return sequence from the memory agent on a fourth plurality of lanes responsive to the second training sequence according to a second mapping.

18. A method according to claim 17 wherein the second plurality of lanes are the same as the fourth plurality of lanes.

19. A method according to claim 18 wherein the lanes comprise bit lanes.

20. A method according to claim 17 wherein the first return sequence comprises one or more groups that are substantially the same as one or more groups in the first training sequence.

21. A method according to claim 17 wherein the second return sequence comprises one or more groups that are substantially the same as one or more groups in the second training sequence.

22. A method according to claim 17 wherein the first training sequence comprises a mapping indicator.

23. A method according to claim 17 wherein the first training sequence comprises an electrical stress pattern.

24. A method according to claim 17 wherein the memory agent comprises a memory module.

25. A method according to claim 17 wherein the memory agent comprises a memory buffer.

26. A memory system comprising:

memory agent comprising:

a first link interface having a plurality of first lanes; and

a second link interface having a plurality of second lanes;

wherein the memory agent may selectively map one or more of the first lanes to one or more of the second lanes; and

a memory controller coupled to the memory agent.

27. A memory agent according to claim 26 wherein:

the first link interface comprises a receive link interface; and

the second link interface comprises a transmit link interface.

28. A memory agent according to claim 26 wherein:

the first lanes comprise receive bit lanes; and

the second lanes comprise transmit bit lanes.

29. A memory system according to claim 26 further comprising a second memory agent coupled to the memory agent.